Code: IT3T1

II B.Tech - I Semester–Regular/Supplementary Examinations
November 2019

DIGITAL SYSTEM DESIGN
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Define binary coded decimal code.
b) Convert the following in to corresponding number systems $(367.52)_8=(\ \ )_2$ and $(AF9.EB)_{16}=(\ \ )_2$
c) Compare between Digital Logic Gate and Integrated Circuit.
d) Minimize the Boolean function F= X’Y’Z+X’YZ+XYZ.
e) Define combinational circuit.
f) Explain a magnitude comparator with considering suitable example.
g) Write minimum steps must be considered for transferring a stored word out of memory.
h) Derive the excitation table of JK and T-flip flops.
i) Write short notes on PLD’s.
j) Define State Table and State Diagram.
k) What are the drawbacks of ripple counters?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2\. a) Perform the following Number base conversions and find out as follows:

(i) $(92.714)_{10} = (\quad)_8$ and (ii) $(41.513)_8 = (\quad)_{10}$ 8 M

b) i) Obtain the 2's complement for the following

a)11011010 b) 01110110

ii) Obtain the 9's complement for the following

a) 12345678 b) 24681234 8 M

3\. a) Obtain minimal expression for $F = \Sigma (1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$ using K – map method. 8 M

b) Simplify the Boolean function $F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$ which has the don't care conditions

$d(w, x, y, z) = \Sigma(0, 2, 5)$ 8 M

4\. a) Write the truth table of 3 bit gray to binary code conversion. Show the realization using 4X1 MUX? 8 M

b) Design full adder and construct with half adders and implement full adder only with NAND gates. 8 M

5\. a) Implement the following Boolean functions using PAL. Also write the PAL programming table.

(i) $F_1(A, B, C, D) = \Sigma$ (6, 8, 9, 12,13,14,15)

(ii) F_2 (A, B, C, D) = Σ (1, 4,5,6,7,10,11,12,13)

(iii) F_3 (A, B, C, D) = Σ (4,5,6,7,10,11)

(iv) F_4 (A, B, C, D) = Σ (4,5,6,7,9,10,11,12,13,14,15) 8 M

b) Realize the following Boolean functions using a PLA.

(i) $F_1 = \Sigma$ (0, 4, 7)

(ii) $F_2 = \Sigma$ (1, 3, 6)

(iii) $F_3 = \Sigma$ (1, 2, 4, 6) 8 M

6. a) Design a Sequential Circuit that detects a sequence of three or more consecutive 1's in a string using D flip flop. 8 M

b) Convert the T-flip flop to function like a JK-flip flop. 8 M